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Improved general purpose communication receiver

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SUMMARY

The EC958/7 is the latest development of the Eddystone 958 l.f/m.f/h.f communication receiver. It combines simple free tuning over 100kHz steps with exceptional frequency stability, drifts of 3 to 4Hz being the maximum under typical working conditions. Free tuning over a larger range with reduced stability is also possible.

To take the most advantage of the enhanced stability on the h.f ranges, a digital display is provided which accurately shows the five least significant figures of the tuned frequency with a resolution of one hertz.

The methods used to achieve this high level of stability are described in particular detail. The design of the free running interpolation oscillator, its characteristics under conditions of vibration and both constant and changing ambient temperatures, the logic system used to translate its frequency to that which the receiver is tuned, all form the basis of this article.

FACTOR DE INTERRUPCIÓN DE RECEPCIÓN DEL RECEPTOR DE ALTA FRECUENCIA:

Sumario

El EC958/7 es el último desarrollo del Receptor de Comunicaciones Eddystone 958 l.f/m.f/h.f. Une una sintonización libre sencilla sobre pasos de 100kHz con una estabilidad de frecuencia excepcional, ya que las variaciones de 3 a 4Hz son las máximas en condiciones de trabajo típicas. También es posible una sintonización libre sobre una amplia gama con reducción de la estabilidad.

Para aprovechar al máximo la ventaja de la acrecentada estabilidad de las gamas de alta frecuencia, se provee un dispositivo de representación visual digital que muestra con precisión los cinco números menos significativos de la frecuencia sintonizada de un Hz.

Se describen con particular detalle los métodos que se han usado para conseguir este alto nivel de estabilidad. El diseño del oscilador continuo de interpolación, sus características en condiciones de vibración y temperaturas ambientales tanto constantes como cambiantes, el sistema lógico que se ha usado para transformar su frecuencia en aquella con la que el receptor está sintonizado, todo esto forma la base de este artículo.

EMPFANGSAUSFALLFAKTOR: VON H.F-EMPFÄNGERN:

Zusammenfassung

Der EC958/7 ist die neueste Entwicklung des Kommunikationsempfängers Eddystone 958 für nieder, mittel und hochfrequensen. Er vereint eine einfache, freie Abstimmung in Stufen von 100kHz mit ausgezeichneter Frequenzstabilität, wobei Abtriften von 3 bis 4Hz unter typischen Betriebsbedingungen Maximalwerte sind. Eine freie Abstimmung über einen größeren Bereich mit geminderter Stabilität ist ebenfalls möglich. Um die verbesserte Stabilität der H.F-Bereiche weitgehendst zu nutzen, hat das Gerät eine Digitalanzeige, die genau die fünf unbedeutendsten Zahlen der abgestimmten Frequenz mit einer Auflösung von einem Hertz zeigt. Besonders genau werden die Methoden beschrieben, die verwendet werden, um diese hochgradige Stabilität zu erreichen. Die Konstruktion des freilaufenden Interpolationsoszillators, seine Eigenschaften unter Vibration sowie konstante und sich ändernde Raumtemperaturen, das

logische System, das zur Übersetzung der Frequenz eingesetzt wird, auf die der Empfänger abgestimmt ist, sind alle Grundlagen des Artikels.

FACTEUR DE DÉFAILLANCE DE RÉCEPTION D'UN RÉCEPTEUR H.F:

Résumé

Le récepteur EC958/7 représente la version la plus récente du récepteur de communications Eddystone 958 l.f/m.f/h.f. Ce nouvel appareil est caractérisé par la simplicité de son accord par gradins de 100kHz et par une stabilité de fréquenc exceptionnelle, les écarts maximum étant de l'ordre de 3 à 4kHz en service normal. L'accord libre sur une gamme plus étendue avec stabilité réduite est également possible.

Pour profiter au maximum de la stabilité améliorée des gammes H.F, un système d'affichage numérique donne avec précision les cinq chiffres les moins significatifs de la fréquence accordée avec une résolution de un Hz.

Les méthodes appliquées pour obtenir ce niveau élevé de stabilité sont décrites en détails. Cet article décrit la conception de l'oscillateur d'interpolation à fonctionnement libre, sa tenue aux vibrations, ses caracteristiques sous températures ambiantes constantes et variables ainsi que le système logique utilisé pour convertir sa fréquence à celle sur laquelle le récepteur est accordé.

INTRODUCTION

The new /7 version of the Eddystone EC958 l.f/m.f/h.f communication receiver is designed to the general specification of useable 1Hz resolution (above 1.6MHz) combined with simple free tuning. This new model is based on the standard 958 receiver, the best features of which have been retained.

To meet the specification, new oscillators are incorporated together with a digital readout, the five least significant figures of the frequency of tune having a resolution of one hertz when the receiver is used on its h.f ranges. Part of the original optical display system is retained for use on the l.f and m.f ranges and for indicating the three most significant figures of the frequency of tune on the h.f ranges. The h.f, m.f and l.f display can be clearly seen in figure 1.

The mechanical construction of the oscillators in particular, and the receiver in general, is designed so that the frequency stability, under vibration conditions, meets the specifications for a receiver in the main region of major and minor warships, as detailed in Defense Specification DEF133.

GENERAL DESCRIPTION

The overall block schematic of the receiver is shown in figure 2. The r.f stage comprises two f.e.t's in a cascode amplifier which precedes a dual-gate m.o.s/f.e.t first signal mixer. Front end selectivity above 53kHz is provided by bandpass input circuitry whilst below this frequency, sufficient protection is afforded by a single tuned circuit.

In the frequency range 1.6 to 30MHz the

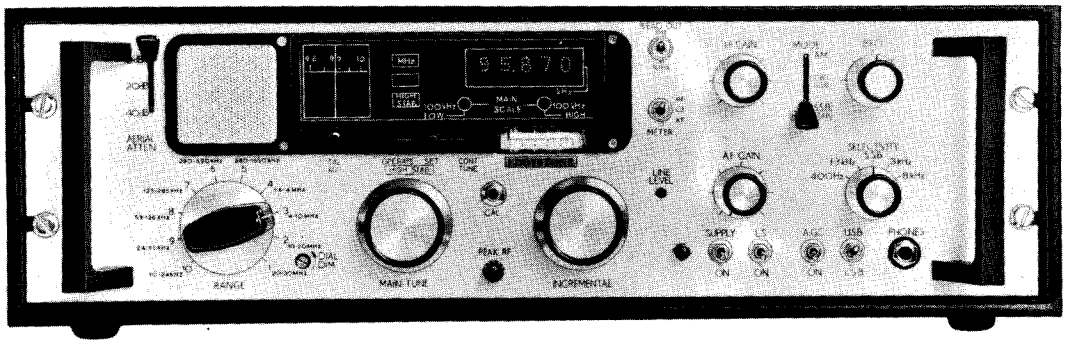


Fig. 1. Front panel of the Eddystone EC958/7 receiver showing the new digital readout

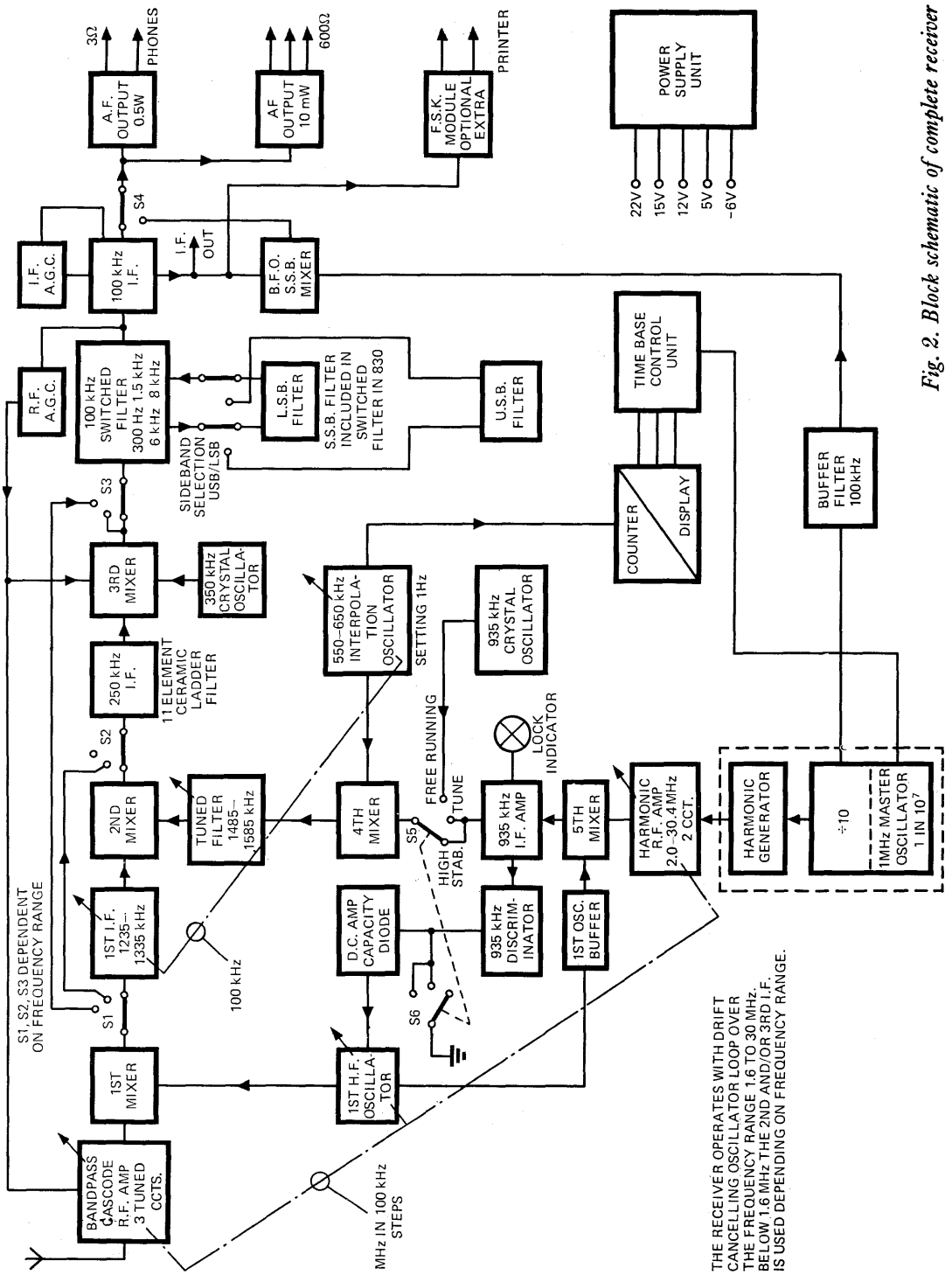


Fig. 2. Block schematic of complete receiver

h.f oscillator is locked in 100 kHz steps to the high stability master oscillator which itself has improved stability so that the accuracy of the receiver, especially at the h.f end of the range, is not impaired.

The overall frequency stability during high stability working is decided by the interpolation oscillator which allows incremental tuning between the 100kHz lockpoints, in conjunction with the tuneable first i.f amplifier.

The 958/7 incorporates a new design of interpolation oscillator comprising a compact, simple h.f oscillator in a solid, temperature controlled box, the required range of frequencies being generated by a fixed divider and filter network.

The setting of the interpolation oscillator is shown by a five digit counter which replaces the original analogue scale display and allows frequency setting to an accuracy of ±1Hz. The counter is programmed to convert the frequency of the oscillator to the tuned frequency of the receiver.

The 250kHz i.f amplifier is the second i.f when operating on the h.f ranges and the first i.f when operating on some of the l.f/m.f ranges.

This unit provides wideband selectivity with an eleven element ceramic ladder filter and conversion to a 100kHz band by means of the third signal mixer m.o.s/f.e.t and the 350kHz oscillator. In common with the other oscillators in this new version of the 958, the stability of the 350kHz oscillator has been improved by temperature controlling and a new design of oscillator circuit.

The main selectivity of the receiver is determined by the five position 100kHz filter whilst sideband selection for s.s.b working is by separate quartz u.s.b/l.s.b filters.

The 100kHz i.f amplifier preceded by the 100kHz filter provides the main gain block of the receiver. The unit comprises detectors for r.f as well as i.f a.g.c, a low impedance i.f output and an a.m detector. The s.s.b detection is by separate b.f.o and product detector. Audio outputs are provided for external speaker and line operation.

The power supply in the 958/7 has been extensively redesigned. The oscillators and t.t.l circuitry in particular, require well regulated voltage supplies. These are provided by the new power supply incorporating integrated circuit regulators in the appropriate lines. This power supply ensures that the frequency stability of the receiver is not affected by mains power supply fluctuations and different load currents within the receiver itself.

A more detailed look at the interpolation oscillator and counter will now be given, as these two items embody many interesting features.

THE INTERPOLATION OSCILLATOR

The interpolation oscillator (i.o) generates the 550 to 650kHz drive to the 2nd loop mixer that is necessary to cover the 100kHz sections between locking points of the drift cancelling loop. The stability of this oscillator largely determines the medium and short term stability of the receiver.

DESIGN AIMS AND APPROACH

Six basic specifications had to be met in the design of the oscillator, these are:

(*a*) A frequency range of approximately 546kHz to 654kHz to provide the 100kHz range with 4kHz overlap at each end.

(*b*) An output level and impedance that would drive 100mV r.m.s into a balanced mixer of 1kΩ input impedance as well as driving a second identical mixer, via several feet

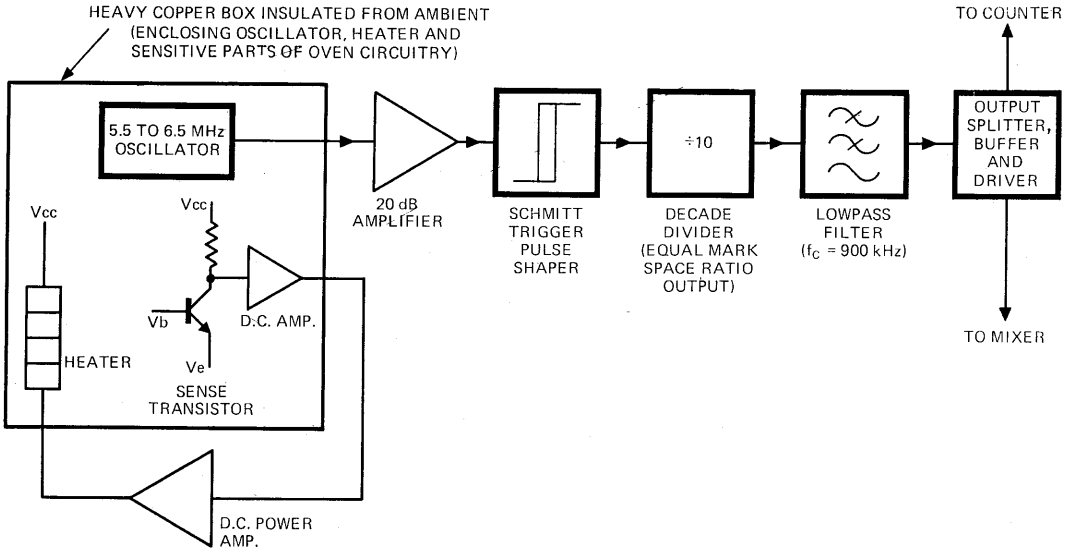


Fig. 3. Block schematic of interpolation oscillator

of coaxial cable, in a second receiver so that two receivers may be used for diversity operation if required.

(*c*) A frequency stability, with constant ambient temperature, in the order of three to four hertz per hour after the oscillator has been switched on for some two hours with further improvements in the drift occurring after this time.

(*d*) A frequency stability, with changing ambient temperature, as high as possible within the physical limitations of the space available in the receiver. An initial figure thought suitable for the first oscillators was 1Hz/°C with a thermal delay, or time constant of the oscillator, mounted in the receiver, of between half and one hour.

(*e*) A frequency stability, under vibration, sufficient to enable the receiver to meet the vibrational specifications for a receiver in the main region of major and minor warships as detailed in Defense Specification DEF133. This required frequency shifts of less than 4Hz peak to peak amplitude for a variety of vibration frequencies and amplitudes.

(*f*) An extra output of about 300mV r.m.s to drive the frequency counter. This is to be at a low impedance and adequately buffered from the output to the mixer to prevent 'spillback' from the counter to the signal circuits.

The specifications are met by the oscillator outlined, in block form, in figure 3. A compact 5.5 to 6.5MHz oscillator is enclosed in an insulated heavy copper box with its temperature closely controlled by a heater coupled to a sensitive temperature dependent device inside the box. A well buffered low impedance, low level output is taken from this oscillator to an amplifier and t.t.l Schmitt trigger. This provides suitable drive for a t.t.l decade divider which generates the required 550 to 650kHz range of frequencies as the oscillator covers the range 5.5 to 6.5MHz. A six pole lowpass filter restores the required sine wave from the square wave

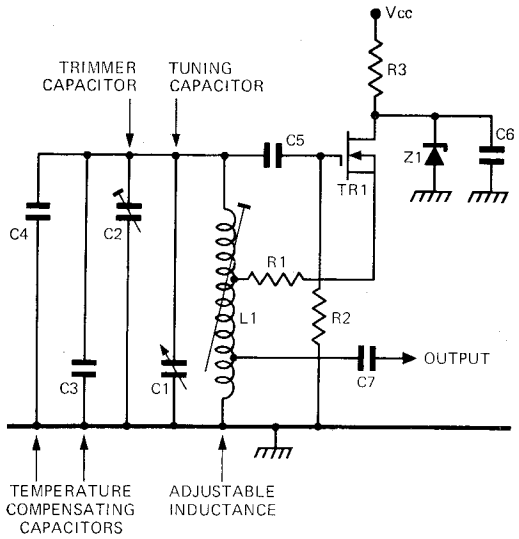


Fig. 4. Circuit diagram of 5.5 to 6.5MHz oscillator

output of the divider whilst a transistor provides isolation between the required outputs and suitable drive levels and impedances to meet the specifications.

5.5 TO 6.5MHz OSCILLATOR

All components which determine the overall frequency of the i.o are situated in the temperature controlled 5.5 to 6.5MHz oscillator unit the circuit of which is shown in figure 4. This range was chosen so that the physical size of the variable capacitor, inductance, etc is kept as small as possible facilitating good temperature control (i.e small unit size keeping temperature gradients to a minimum). The use of this frequency range also enables a rigid single layer inductance, Ll, to be used rather than the bulky wave-wound inductance required for a basic 550 to 650kHz oscillator. An internal view of the basic oscillator is shown in figure 5.

The active device is a single gate m.o.s/f.e.t of good parameter stability (gate-source capacitance, etc). To enhance this stability, degenerative source feedback is applied by resistor R1 at a.c and d.c.

Positive feedback is applied via a tap on the inductance Ll, the oscillator output being taken from a second tapping point which is at a very low impedance thus ensuring that loading effects on the output do not change the frequency to any great extent.

The supply voltage of the oscillator is further regulated by Zener Z1. The resulting stability of the oscillator, with changing supply voltage, is less than $\pm$ 100Hz for a supply voltage change of $\pm$ 1V from the normal 12V.

Each oscillator is individually temperature compensated by using the appropriate ratio of negative temperature coefficient ceramic and positive temperature coefficient silver mica capacitors as tank capacity.

All components are of high quality; metal film resistors, silver mica and scintillation free ceramic capacitors being used. Components which might move under vibration are semi-encapsulated in Araldite and when tested, the box in which the oscillator board is mounted is soldered together to prevent any tendency to 'open'.

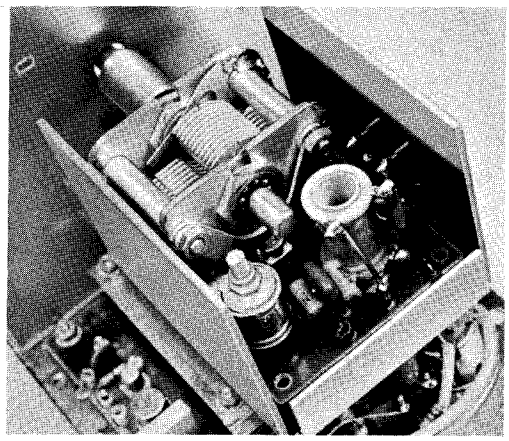


Fig. 5. Internal view 5.5 to 6.5MHz oscillator showing the simple design using the minimum number of critical components

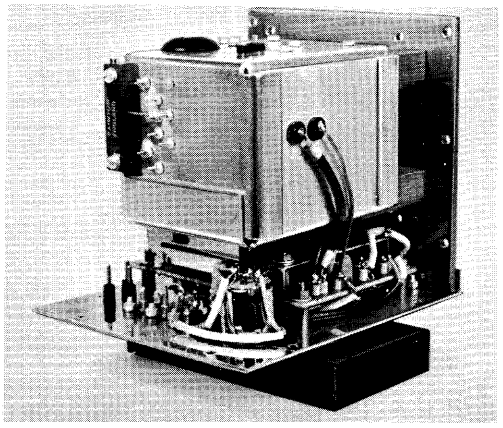


Fig. 6. View of interpolation oscillator with cover and thermal insulation removed, showing the box, frequency divider and filter board

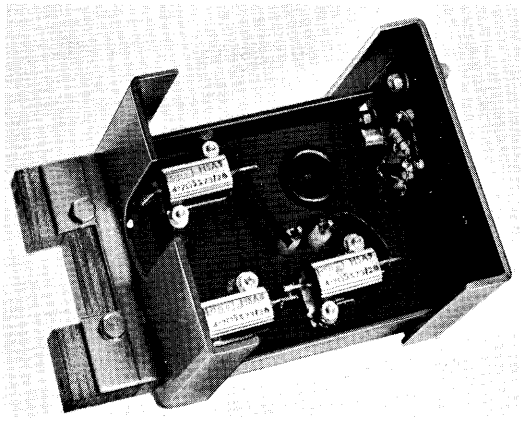


Fig. 7. View of top section 5.5 to 6.5MHz oscillator, showing heating elements and temperature sensing circuitry

A comprehensive test procedure for this unit has been formulated which ensures that every 5.5 to 6.5MHz oscillator meets the stringent specification and for reliability reasons, some of the more critical parts of the construction are performed by the test engineer during these tests.

THE DIVIDER UNIT

This is a non-critical section of the interpolation oscillator unit where variation in the parameters of the devices used do not affect the frequency stability, consequently no temperature control is necessary. It is, however, double-screened to prevent radiation of harmonics and the fundamental of the square-waves present in the t.t.l circuitry.

The logic level square wave, after filtering, provides a very constant level of oscillator drive of sufficient purity to keep spurious responses, etc well within the original specification, i.e $< 1\mu$V equivalent signal (e.m.f from 50Ω) at the antenna.

The divider unit is shown in figure 6 which is a photograph of the complete unit.

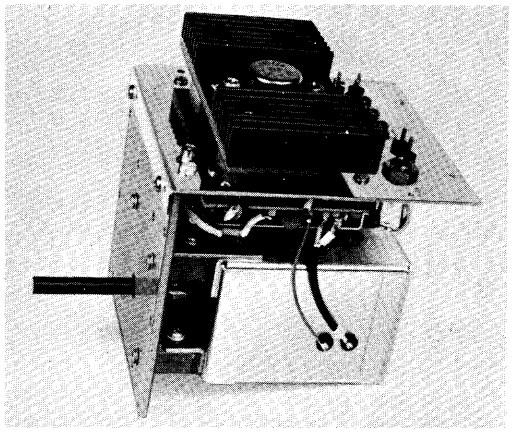


Fig. 8. View of interpolation oscillator with cover and thermal insulation removed, showing top connections and proportional oven power amplifier

OVEN CIRCUITRY

The temperature sensing device is a transistor mounted in the 5.5 to 6.5MHz oscillator unit. The approximate -2mV/°C Vbe characteristic change of the transistor is amplified by a two stage transistor amplifier (super α pair followed by a common emitter power amplifier stage mounted outside the interpolation oscillator unit) which drives current through the power resistor heater elements mounted

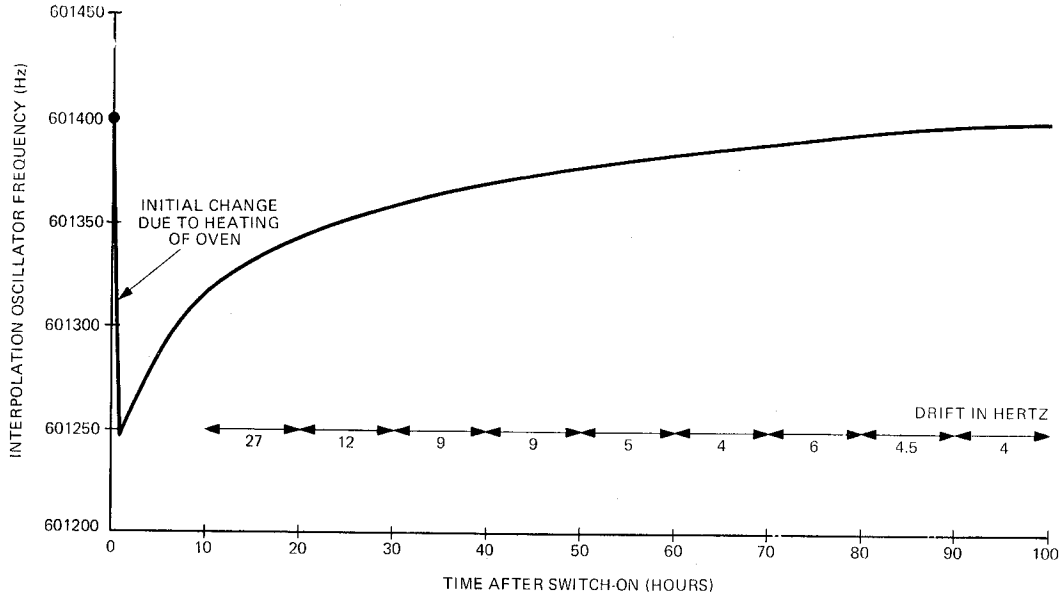


Fig. 9. Interpolation oscillator 100 hour stability test figures

in the heat-sink clamped on the 5.5 to 6.5MHz oscillator box. The heaters and sensor transistor can be seen in figure 7 and the power amplifier in figure 8. The temperature is set by the d.c voltage applied to the base of the sensing transistor to a value in the range 65 to 70°C. The resulting long term temperature stability is very good with only small short term variations because of the proportional heating nature of the oven circuitry.

The heat loss is kept low by the use of conventional insulating material around the 5.5 to 6.5MHz oscillator box with bright-plating and matt-blacking on appropriate surfaces.

PERFORMANCE OF A TYPICAL INTERPOLATION OSCILLATOR

The long term stability, temperature stability and performance of the whole 958/7 receiver under vibration conditions is shown in figures 9, 10 and 11.

The constant ambient long term stability settles to 4Hz/h after 10h, less than 2Hz/h after 20h and less than 1Hz/h after 30h. These figures show that extremely high stability can be achieved when the receiver is in semi-permanent use in a moderately constant ambient. In view of this, the receiver is provided with a switch for removing the power to all the circuits except the actual oscillators.

The temperature stability shown in figure 10 is for the oscillator alone, removed from the receiver. Since aging drift and temperature drifts are very similar, they have to be separated graphically as shown. This is done by operating the unit in a constant ambient until a steady aging drift is obtained. The ambient temperature is then increased causing the frequency to alter from the steady aging rate before returning to it after a period of time when the full effects of the temperature rise have been absorbed. The new aging rate will have commenced at a constant frequency shift from the extrapolation of the lower

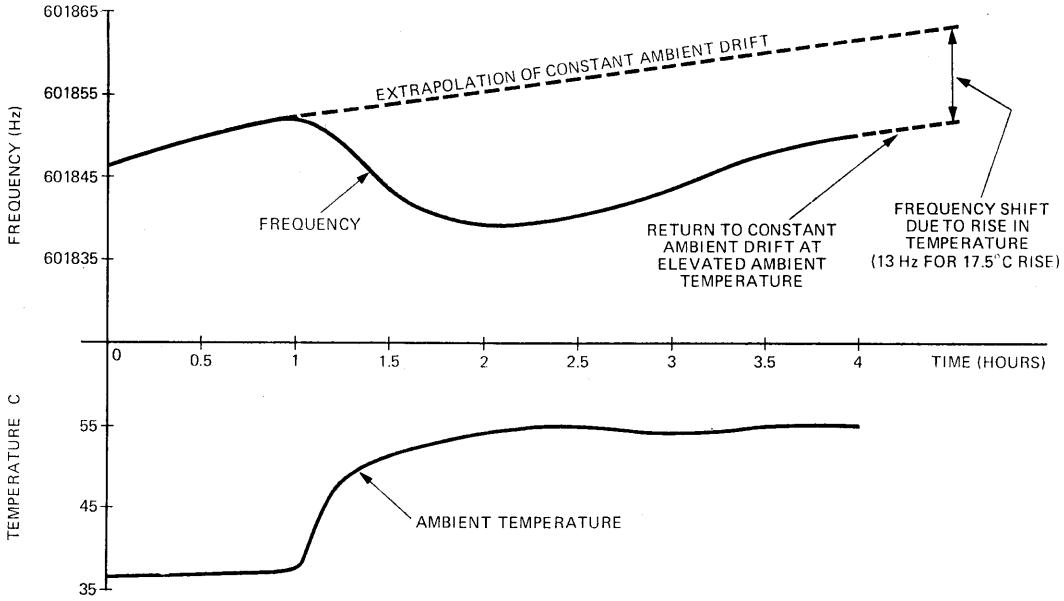


Fig. 10. Interpolation oscillator ambient temperature/frequency drift test figures

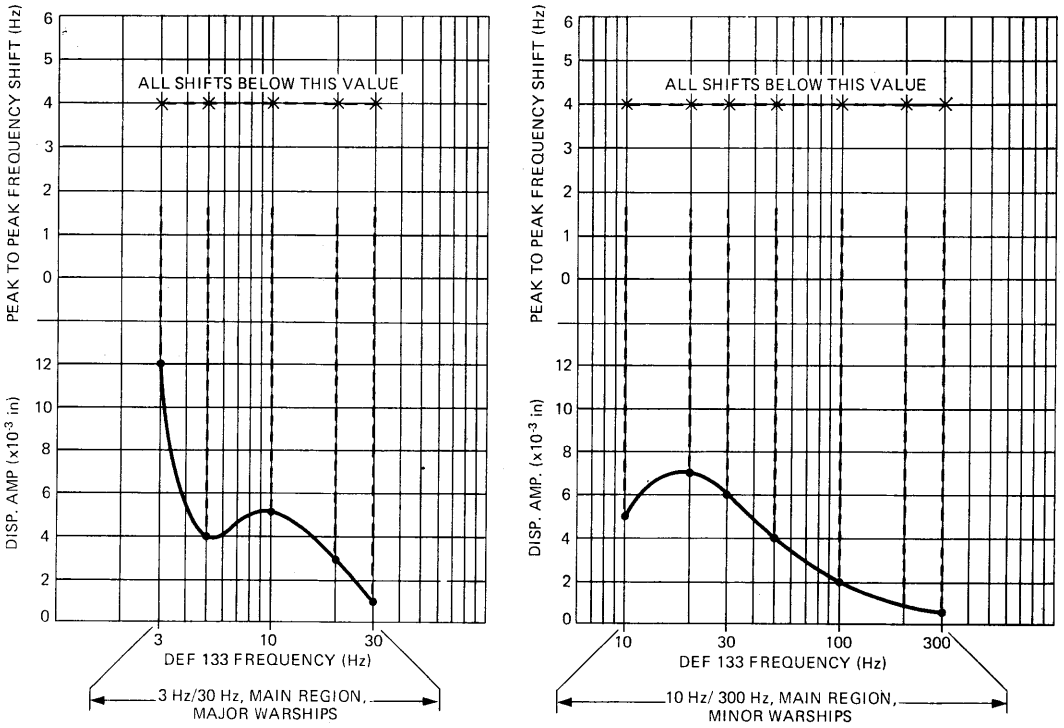


Fig. 11. Results of DEF 133 vibration tests

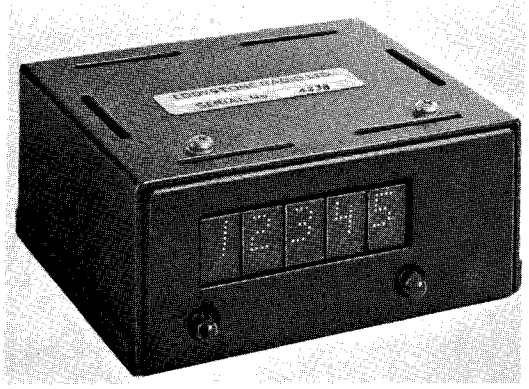


Fig. 12. Outer view of counter/display assembly showing the L.E.D display and the 'read main scale' lamps

temperature aging rate. This shift is the frequency shift caused by the temperature rise and figure 10 shows this to be approximately 13Hz for a 17.5°C rise, i.e <1Hz/°C temperature coefficient. When the unit is mounted in the enclosed receiver a thermal delay is introduced with a similar overall temperature coefficient.

The performance of the receiver mounted on suitable shock mounts, under the vibration conditions as specified in DEF133 is shown in figure 11. All the resulting shifts were well below the 4Hz peak-to-peak limit, being too low to be measured accurately with the currently available equipment.

THE COUNTER

The frequency of the interpolation oscillator is displayed by the counter which has a built-in offset to convert the range 650–550kHz to 0–100kHz so as to be compatible with the main scale 100kHz lock points. The counter is in two parts – the counter/display assembly, figures 12 and 13, and the timebase unit, figure 14.

The counter replaces the optical display disc calibrated 0–100kHz and occupies a space of $80 \times 42 \times 95$mm ($3.15 \times 1.65 \times 3.74$in).

Although the interpolation oscillator tuning range is only 100kHz, an overlap of 4kHz is provided at each end to facilitate tuning at the ends of the ranges. This was originally catered for on the optical display as 'below 0' $-1 \ldots -2$ etc and 'above 100' as 101...102 etc. In the new design of the counter, both these problems have been solved rather differently. The 'below 0' condition, to be compatible with the optical disc, would have required the counter to change direction going through 0 and a minus sign to be displayed. This would be both confusing and complex. The solution chosen is to let the counter go to 99, i.e at -1, 98 at -2, etc and a flashing light shows up indicating that the main scale reading should have 100kHz subtracted from it. The 100 and above condition would have required an extra digit to be shown but this was felt to be confusing as the interpolation reading must always be added to the main scale reading for any particular received frequency. To avoid confusion 100... 101... 102 are now shown as 00... 01... 02... and another flashing light indicates that 100kHz must be added to the main scale reading. The counter/display

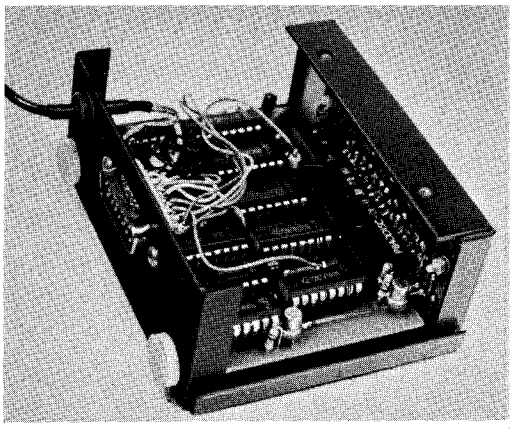


Fig. 13. Internal view of the counter/display assembly showing the compact construction

therefore is a 5 digit system displaying 00.000–99.999 with separate plus and minus 100kHz indication. The counter may be switched to display readings to 1Hz or 10Hz as is most suitable.

A few notes on some of the design problems associated with the foregoing requirements of the new counter will be of interest. In order to convert the 650–550kHz from the interpolation oscillator to '0–100' on the display, two separate conditions must be fulfilled:

(1) The frequency 'direction' must be changed

(2) An offset is required such that 650 = 0 and 550 = 100.

By the inversion property of a mixer the first condition may be obtained, i.e mixing the interpolation oscillator frequency with 1MHz from the master oscillator. This produces the required frequency direction but also increases the spurious responses being picked up by the receiver as a whole. The solution adopted is to use six reverse counting presetable decades to drive the display which solves both (1) and (2) conditions. Referring to figure 15 the operation is as follows. The output from the interpolation oscillator is amplified and shaped to logic level and gated for 1s or 100ms depending whether display is to be 1Hz or 10Hz. The output from the signal gate is applied to the 1Hz decade and from this to the 10Hz, 100Hz decades and so on through six decades. For example, consider the case of 650kHz applied to this counter. The six decades have been preset to 650000 so that on opening the signal gate the counter starts to count backwards – 649999, 649998, 649997...to 000000 after 1 second. If 550kHz is applied, the same sequence occurs – 649999, 649998, 649997...to 100000. The required frequency 'direction' (1) and the required offset (2) is therefore obtained.

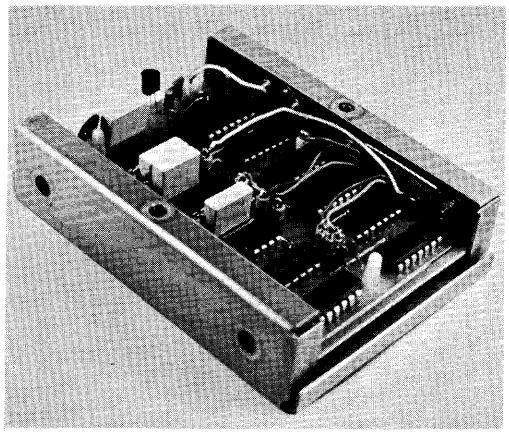


Fig. 14. Internal view of the timebase unit

The count information is applied in b.c.d form from five reverse counting, presetable decades to the displays as shown. The information from the preset to six decade is used to drive the read main scale plus or minus 100kHz lamps. The output from this decade is fed into the 9–0–1 decoder which recognizes one of the three states the counter could be in:

(*a*) 0 – Count must be between 000.000 and 099.999, action taken, none.

(*b*) 9 – Count must be 999.999 or less, an output is taken via a latch to the read main scale – 100kHz lamp.

(*c*) 1 – Count must be 100.000 or above, an output is taken via a latch to the read main scale + 100kHz lamp

In order to provide an effective warning the 'read main scale lamps' are flashed during operation by strobing the latch output with the 1s or 100ms clock pulses in the 'blink gate'.

THE DIGITAL DISPLAY

The count must be displayed in an 'on-line', i.e static fashion, only being changed if the count information is changed. This requires a latch and decoder between each display

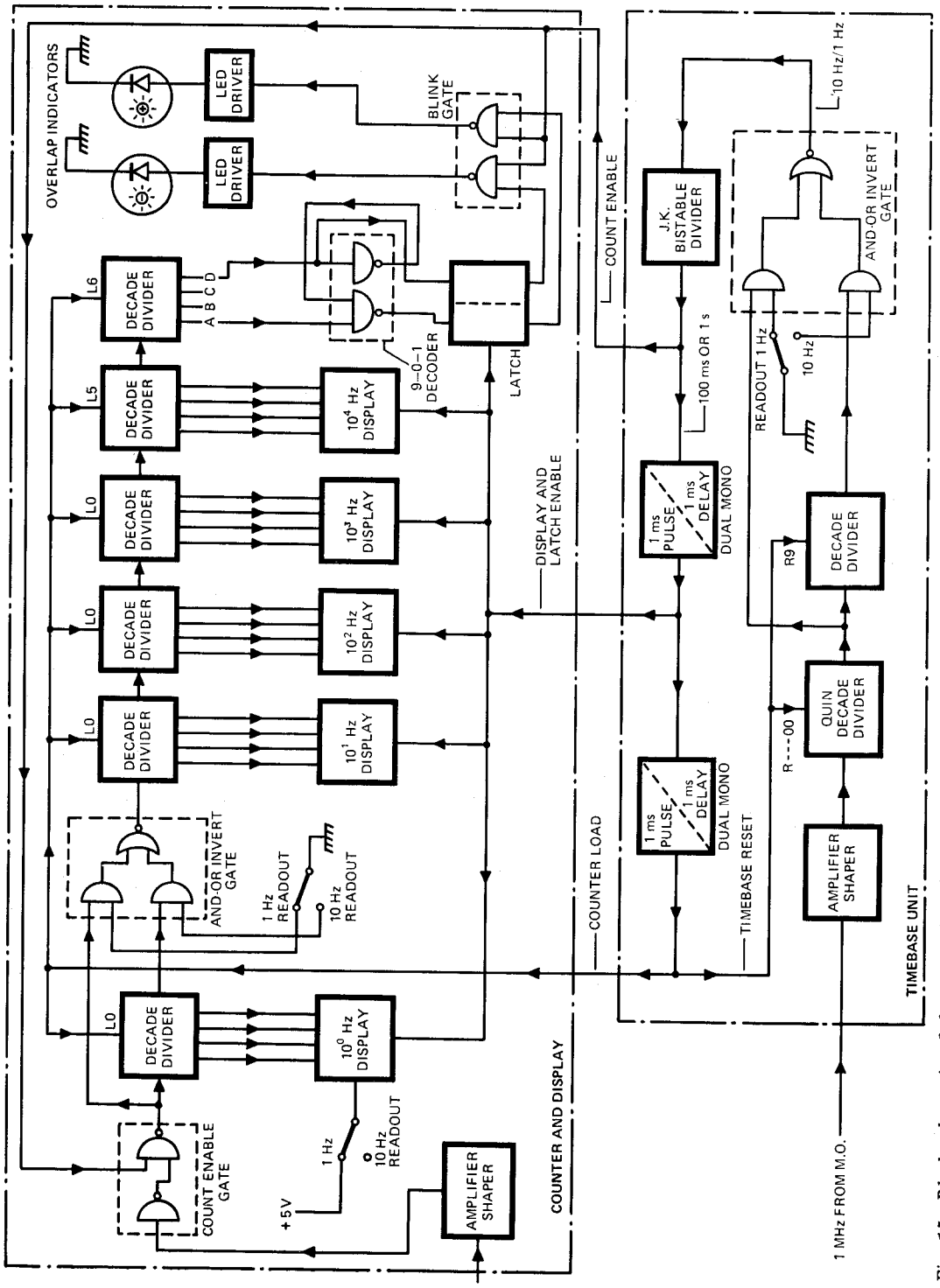


Fig. 15. Block schematic of the counter/timebase arrangement

which could mean up to ten separate i.c's just to display the count information. In order to capitalize on the space available it was decided to opt for an L.E.D digital display with integral latch and decode facilities. The display selected is a 7×4 dot matrix type with the latch and decode circuitry on an m.s.i chip at the base of the display. The figure dimensions are $7{,}4 \times 4{,}9$mm (0.29×0.19in). It is only necessary to supply each display with b.c.d information from the counter and latch timing information from the timebase.

The complete counter/display assembly comprises two boards connected by a 30-way edge connector and ten flying leads to a socket mounted in the counter box carrying control information from the timebase.

THE TIMEBASE UNIT

This unit (figure 14) provides four sequenced control signals to the counter with the radiation around the receiver being kept to a minimum. Referring to figure 15, a frequency of 1MHz at 30mV derived from the master oscillator, is amplified and shaped to logic level. It is applied to a Schmitt trigger which provides a fast edge to drive the first decade divider in a chain of six. The 1Hz output is converted to a 1s pulse by a J-K bistable and this output is used to open the signal gate on the counter to enable the count. The falling edge of this count enable pulse starts a chain of cascade connected monostables – the falling edge of one starts the next one. The operating sequence is therefore:

(1) Enable count for 1s
(2) Delay for 1ms
(3) Enable display for 1ms
(4) Delay for 1ms
(5) Load counter 650000 and reset timebase.

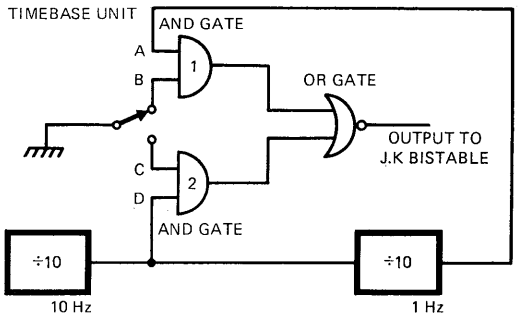
The timebase unit occupies a cube $100 \times 75 \times 28$mm ($3.94 \times 2.95 \times 1.1$in) and interconnection with the counter/display assembly is by screened multiway cable.

The counter displays the interpolation oscillator frequency to 10Hz or 1Hz and this is effected by bypassing a decade in the counter/display assembly and in the timebase unit. The switching – d.c only – is carried out by the AND-OR-INVERT gate. Operation is the same for the counter/display assembly as for the timebase unit and is as shown in figure 16.

The complete counter system is designed with t.t.l and contains a total of twenty integrated circuits.

MASTER OSCILLATOR

The master oscillator generates the reference 1MHz which controls the setting accuracy of the 100kHz points in the drift cancelling loop system. The basic oscillator features a proportionately controlled oven which gives it a frequency stability of ± 0.5 parts in 10^7 over the temperature range 0 to $+50$°C. This is



GATE 1		GATE 2		OUTPUT
A	B	C	D	
1 Hz	0	1	10 Hz	10 Hz
1 Hz	1	0	10 Hz	1 Hz

Fig. 16. Diagram and truth table of the AND-OR-INVERT gate

equivalent to a worst case drift of ±1.5Hz at a 100kHz setting point at 30MHz over the 50°C range.

This oscillator also provides the source for the timebase of the counter unit with an error, over the temperature range, well below the ±1Hz resolution of the counter display.

Any long term aging drift of this oscillator can be corrected by adjustment of a fine trimmer which is easily accessible when the receiver cabinet is removed.

350kHz OSCILLATOR

This is a simple crystal controlled type of oscillator. The crystal is operated in anti resonance with a 30pF load, tapped capacity feedback is used with a m.o.s/f.e.t as the gain element. The crystal is mounted in a proportionately controlled oven which provides the circuit with better than 1Hz stability over the 0 to +50°C range of temperature. To provide a reasonably clean drive the oscillator output is filtered by a single tuned circuit, before being fed to the final mixer.

As with the master oscillator, a fine trimming facility is provided so that any long term aging drift of the crystal can be corrected.

POWER SUPPLY

The widely varying current requirements with ambient temperature changes and range selection demand a high standard of regulation from the power supply.

The 110–250V a.c mains input is converted to 22V d.c for powering the interpolation oscillator oven, −6V d.c for the a.g.c and 12V and 15V d.c for the bulk of the receiver.

The most critical supply rail is the 12V d.c line which not only supplies oscillators but also two crystal ovens. This supply line incorporates an i.c voltage regulator which, via an external pass transistor, produces a very low impedance supply. The circuit also incorporates foldback current limiting as a safety feature, so that in the event of a short circuit developing, the supply current instantly reduces to half its normal value and remains so until the 'short' is removed. The dissipation during this time is less than normal and this feature helps to avoid accidental damage when the receiver is being maintained or adjusted with the supply connected. The voltage regulator effectively isolates the 12V d.c line from any r.f interference on the a.c supply input.

The 15V d.c and −6V d.c lines are derived from separate shunt regulator Zener diodes.

The counter/timebase power supply has an i.c voltage regulator similar to the 12V d.c line as good regulation is essential for t.t.l systems if mis-triggering either from power supply variations or external sources is to be avoided. It is also important that logic level switching transients are not fed back through the supply to modulate other h.t lines within the receiver. It is for this reason that the 5V d.c line is derived from a separate winding on the mains transformer maintaining as much isolation as possible.

Switching the counter and timebase off on the low-frequency bands is performed by using 'remote shut down' of the power supply. Instead of having to switch a current of 1.3A it is necessary only to switch a control current of some 200μA thus obviating the need for heavy duty switch contacts.

The 12V d.c and 5V d.c lines have their power transistors on a 102×94×16mm (4.02×3.7×0.63in) finned heat sink thermally isolated from the back panel. This is to ensure that the heat sink does the work and that the temperature of the rest of the receiver does not rise unduly.

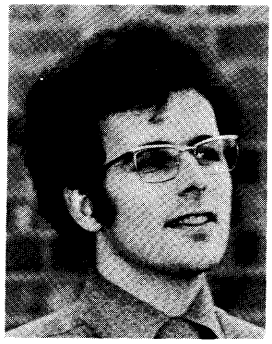
CONCLUSIONS

The latest development of the Eddystone 958 series receiver, the 958/7, whilst retaining all the normal facilities, now provides useable 1Hz resolution. Simple two knob, free-tuning has been provided with an order of stability normally only found in the synthesized receiver bracket. The new digital frequency readout provides unambiguous tuned frequency indication.

To meet the requirement of useable 1Hz resolution the mechanical stability has been improved to comply with the vibrational specification outlined in DEF133. The power supply stability has been improved by the use of voltage regulators and development of an i.s.b facility, at little extra cost, is now possible.

Reference

[1]D. W. FORD: 'Solid-state general purpose receiver – 10kHz to 30MHz', *Point-to-Point Telecommunications*, Vol. 13, No. 1 (January 1969).



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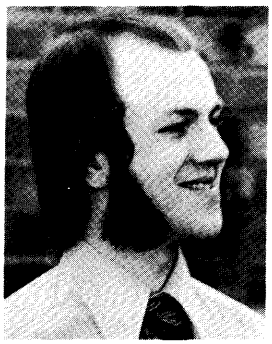

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